Xilinx Virtex 4 LX25 Preliminary Test Results (Effects of NASA/GSFC REAG scrubber)

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Test Date: 3/2006; 6/2006; 7/2006; 8/2006; 8/2007; Report Date: 10/2006

1. INTRODUCTION

This study was undertaken to determine the single event destructive and transient susceptibility of the Xilinx Virtex 4 – LX25. The tests reported in this document are preliminary steps within the full study of the Virtex 4- family. Key objective of the preliminary research was to determine the effectiveness of external scrubbing of the Xilinx V4 SRAM-based FPGA device. The devices were monitored for Single Event Transient (SET) and Single Event Upset (SEU) induced faults by exposing them to a heavy ion beam at the Texas A&M University Cyclotron Single Event Effects Test Facility.

2. DEVICES TESTED

There were several shift register designs with 2 separate scrubbing schemes tested within separate LX25 parts. The devices were manufactured on an advanced 0.9nm copper CMOS Process Technology. The manufacturer is Xilinx.

2.1 DUT Architecture

All DUTS consisted of shift register strings. We started with a length of 10,000 and observed that the duration of time of inoperability was too large upon configuration hits (time to scrub the bit + 10,000 cycles of recovery). Later tests utilized strings of 300 flip-flops with varying layers of combinatorial logic.

2.1.1 Shift Register String Lengths

Test dates 3/2006 to 8/2006 implemented shift register strings of 10,000. Test dates in 08/2007 used shift register strings of 300.

2.1.2 Principle Configuration

The Principle Configuration is a shift register string consisting of varying number of flip-flops (see section 2.1.1). A By-4 clock divider circuit is implemented to shift the last 4 bits of the Shift register string into a DFF window (SCAN_DATA). The window is output to the tester. A

data clock (SHIFT_CLK) is also output to the tester for high speed synchronous data capture. Reset passes through an asynchronous assert – synchronous de-assert circuit and is supplied to every DFF. The following is the reset circuit used within the DUT.

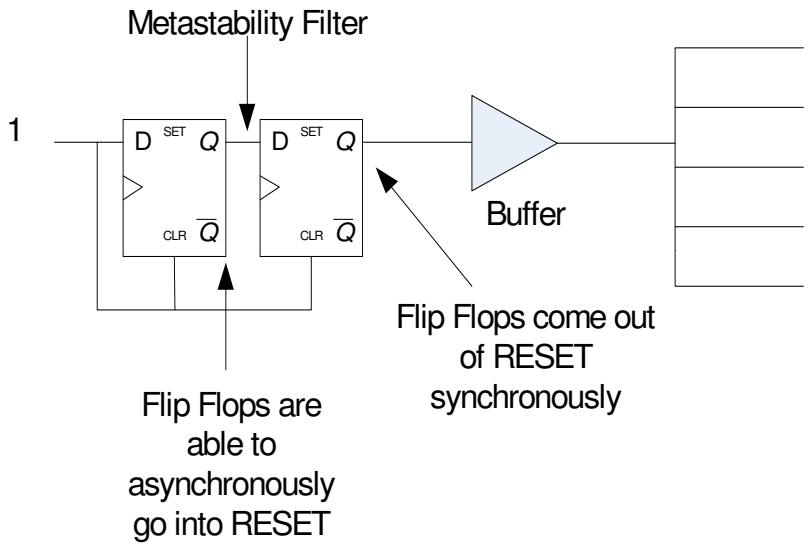

Figure 1: Asynchronous Assert - Synchronous De-assert

Table 1: Device Utilization

LX25 shift register Device Utilization Table Summary			
Logic Utilization	Used	Available	Utilization
Number of Slice Flip Flops	1829	21504	8%
Number of 4 input LUTs	16,625	21504	77%
Logic Distribution			
Number of occupied Slices	9841	10752	91%
Total Number 4 input LUTs	16625	21504	77%
Total equivalent gate count for design	114382		
LX25 shift register Device Utilization Table Summary			
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Number of occupied Slices	9841	10752	91%
Total Number 4 input LUTs	16625	21504	77%
Total equivalent gate count for design	114382		

The following is the DUT configuration schematic:

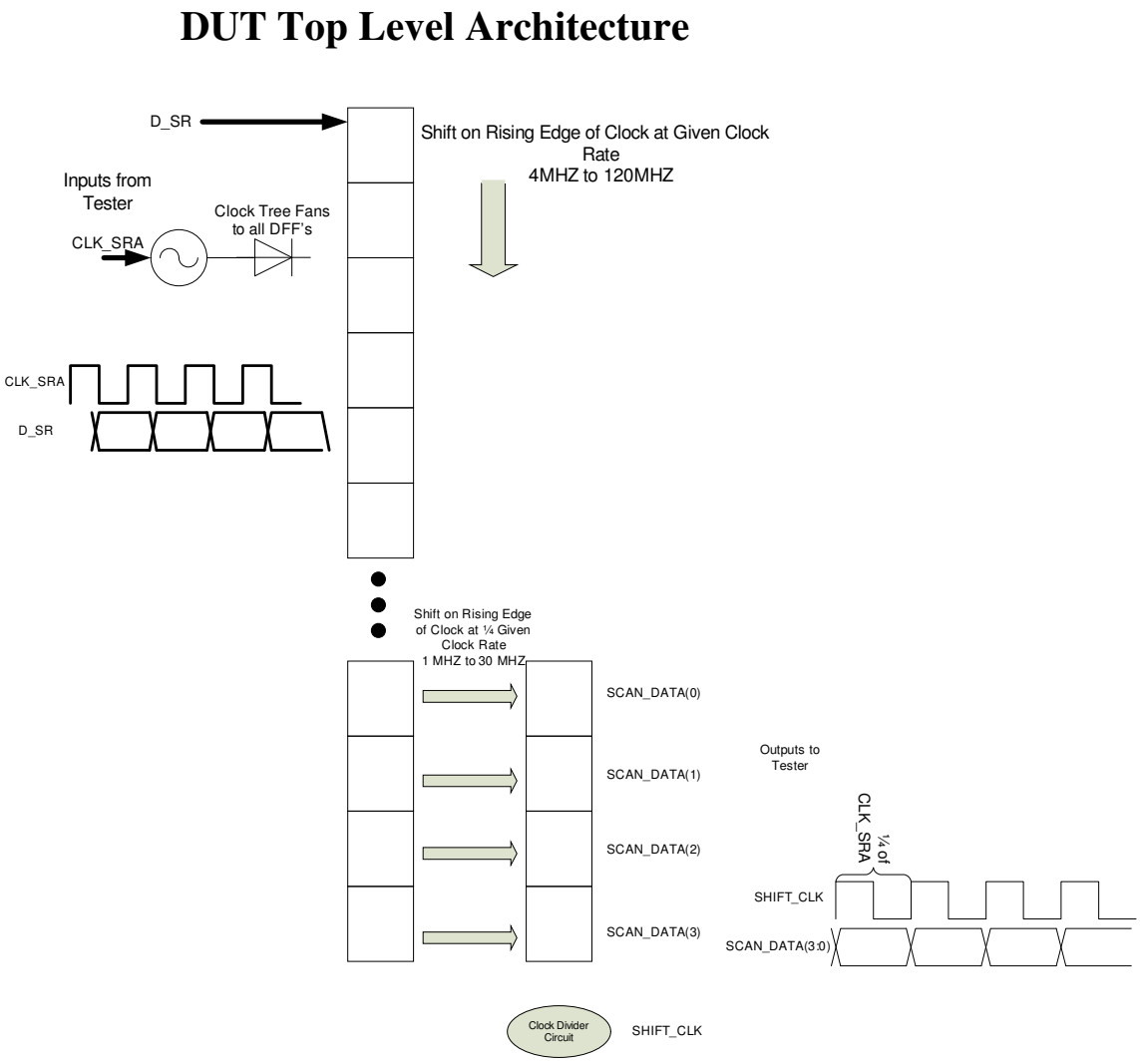

Figure 2: Device Under Test Top Level Architecture

3. TEST FACILITY

3.1 Heavy Ion.

Facility: Texas A&M University Cyclotron Single Event Effects Test Facility, 25 MeV/amu tune).
Flux: 1.0E04 to 2.0E05 particles/cm^2/s
Fluence: All tests were run to 1 x 10^7 p/cm^2 or until destructive or functional events occurred.

Table 2: LET Table

Ion	Energy (MEV/Nucleon)	LET (MEV/cm2/mg) 0 deg	LET (MEV/cm2/mg) 45 deg
Ar	25	5.7	8.5
Cu	25	20.7	
Kr	25	28.5	40.26
Xe	25	52.7	74.5

3.2 Proton

Tests were performed at two facilities.

Facility: Crocker Nuclear Laboratory (CNL) at the University of California at Davis (UCD)
Flux: 1.0E09 particles/cm^2*s
Fluence: All tests were run to 7.14E11 p/cm^2
Energy : 63 Mev-protons

Facility: Indiana University Cyclotron Facility (IUCF)
Flux: 3.0E9 particles/cm2/s
Fluence: All tests were run to 1.0E12 p/cm2
Energy : 195 MeV - incident

4. TEST CONDITIONS

Test Temperature: Room Temperature
Operating Frequency: 15MHz to 100MHz
Power Supply Voltage: 3.3v I/O and 1.5V Core.

5. TEST METHODS

5.1 Architectural Overview

The Virtex-4 LX25 controller/processor is instantiated as a sub component within the Low Cost Digital Tester (LCDT). The LCDT consists of a Mother Board (FPGA Based Controller/Processor) and a daughter board (containing DUT and its associated necessary circuitry). There was a daughter board created for each DUT. The objective of this DUT Controller/processor is to supply inputs to the Virtex-4 LX25 Device and perform data processing on the outputs of the Virtex-4 LX25. The LCDT communicates with a user controlled PC. The user interface is LAB-VIEW. It will send user specified commands to the mother board and receive information from the mother board. Please see Documents: "LCDT" and "General Tester" for further information concerning the LCDT functionality. The LCDT is connected to the Virtex-4 LX25 DUT as shown in the following Block Diagram.

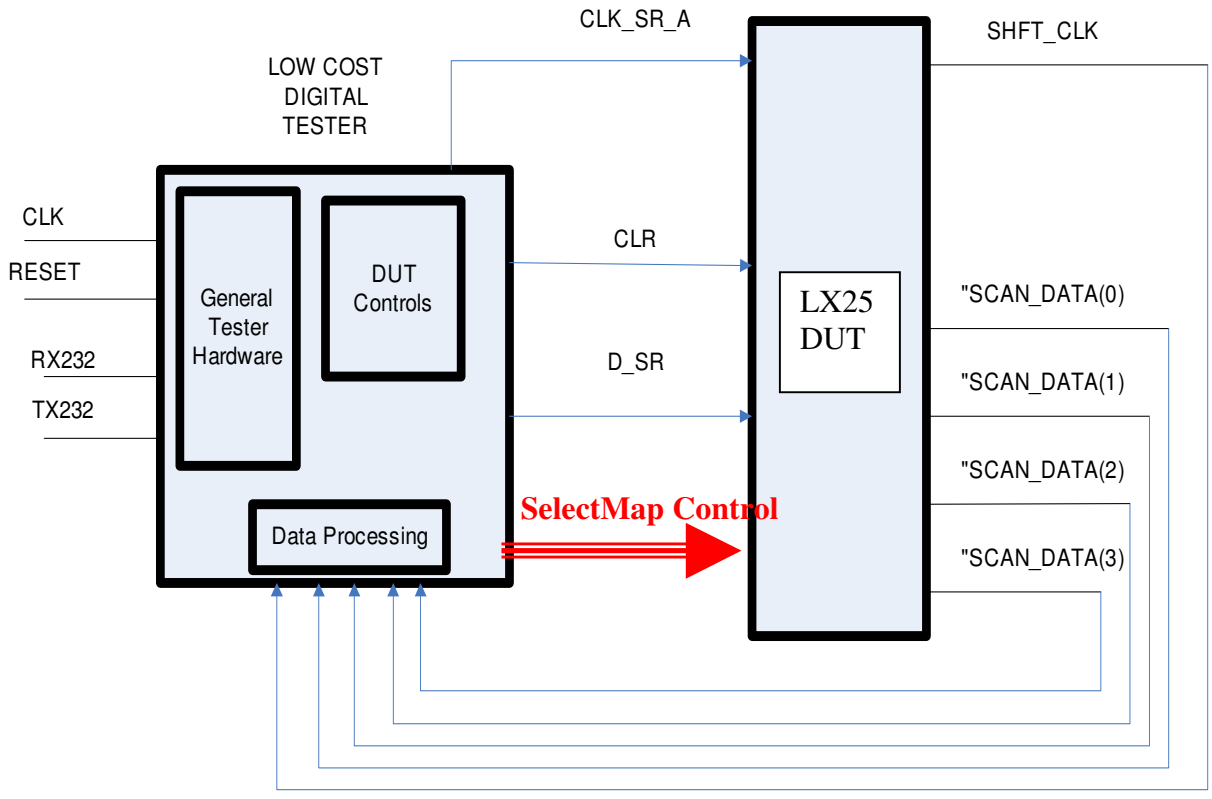

Figure 3: System Level Tester Architecture

5.1.1 Tester I/O List and Definitions

Table 3: I/O Table

Input Name	Description	Direction	Synchronous	Slew	Pullup
CLK	System clock of the LCDT	Input	Clock		N
RESET	LCDT system reset	Input	A		N
RX232	Serial receive input	Input	A		N
SCAN_DATA(4:0)	Data window of Virtex-4 LX25. Data is processed by LCDT and compared against expected value	Input	A		N
SHIFT_CLK	Output clock of VIRTEX-4 LX25. Used to control SCAN_DATA capture. SHIFT_CLK is always ¼ the speed of CLK_SR_A. However it is not synchronous with CLK_SR_A	Input	A		N
CLK_SR_A	Input clock to VIRTEX-4 LX25. Max speed is 150mhz	Output		FAST	N
CLR	Reset to the Virtex-4 LX25	Output		FAST	N
D_SR	Data Input to the Virtex-4 LX25	Output			N
TX232	Serial transmission line	Output			N
Selectmap_CCLK	SelectMap 30MHz clock	Output			

Selectmap_CSN	SelectMap Data valid	Output			
Selectmap_DONE	SelectMap Done (configuration) signal	Output			
Selectmap_BUSY	SelectMap Busy	Output			
Selectmap_INIT	SelectMap INIT	Output			
Selectmap_PROG_B	SelectMap Reset Signal	Output			
Selectmap_RW_B	SelectMap Read/Write	Output			
Selectmap_DATA	SelectMap 8bit Data	Output			
SCRUB_RX232	Serial input to receive configuration data via RS232 port	Input	A		
SCRUB_Tx232	Not Used				
SRAM_D	SRAM Data 16bit	INOUT	A		
SRAM_A	SRAM Address = 20 bits	Output			
SRAM_WR	SRAM read/write	Output			
SRAM_OE	SRAM output enable	Output			
SRAM_CE	SRAM chip select	Output			
SRAM_BLEN	SRAM byte enable	Output			
SRAM_BLHN	SRAM byte enable	Output			
RUN_SCAN	Turn self scrubber on	Output			
SCAN_ACTIVE	Self scrubber	Input	A		
SCAN_ERROR	Self scrubber	Input	A		
SCAN_MODE	Self scrubber	Output			
ERROR_INJECT	Self scrubber	Output			
SEU_DETECT	Self scrubber	Output			
QUICKUSB_FCLK	50MHz clock from	Input	CLK		

	quickusb device				
QUICKUSB_REN		Output			
QUICKUSB_WEN		Output			
QUICKUSB_DATA	8 bit data	INOUT	A		
QUICKUSB_CMD_DATA	Command differentiation	Output			
TP*n*	Test points	Output			

5.2 Requirements

5.2.1 Requirement Summary

There are 3 main investigations:

1. Test shift register logic structures
2. Test external scrubber
3. Test Xilinx internal scrubber

The requirements for the Virtex-4 LX25 LCDT tester are listed in Table 3.

Table 4 – Requirements Table

Item	Requirement
1	Supply System Clock to the Virtex-4 LX25 DUT
2	Supply Reset to Virtex-4 LX25
3	Supply Data Input to the Virtex-4 LX25
4	Clock Frequency of Virtex-4 LX25 shall be variable
5	Maximum Virtex-4 LX25 input clock frequency shall be 100Mhz
6	0,1, and checker board data patterns shall be generated and placed on the VIRTEX-4 LX25 data lines
7	VIRTEX-4 LX25 reset shall be active low

8	VIRTEX-4 LX25 reset shall be active for at least 3 VIRTEX-4 LX25 system clocks
9	VIRTEX-4 LX25 Data Inputs shall be stable at the Rising Edge of the VIRTEX-4 LX25 system clock with a set-up time of 3ns and a hold time of 3ns
10	VIRTEX-4 LX25 data inputs shall be captured by the LCDT data processing module once detecting the rising edge of the data clock (SHIFT_CLK)
11	SHIFT_CLK rising edge detection must include a metastability filter because the SHIFT_CLK input is asynchronous.
12	Input Data must be registered before the data processing block implements the compares – protects against radiation induced I/O transients.
13	Data processing block shall report every error to the FIFO block
14	Tester must supply external LX25 scrubber
15	Tester must be able to control an internal scrubber

The tester supplies inputs as follows: Data (D_SR) changes at the falling edge of the input clock (CLK_SR) so that it is stable and can be captured at the rising edge. CLK_SR and D_SR will be at the user specified frequency. The user will also supply (by command) the preferred data pattern. Data patterns range from all 0's , all 1's, and alternating 1's and 0's.

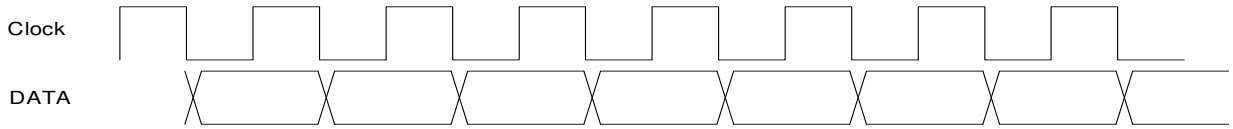

Figure 4: Tester Output to DUT - Clock and Data Relation

5.2.2 External Scrubbing vs. Internal Scrubbing

External scrubber is contained in the tester. It will communicate with the DUT via SelectMap I/O (8 bit). External scrubber is implemented very similar to the DUT configuration manager. Difference between the external scrubber and configuration manager is the command stream and the total number of data bytes to be written.

5.3 User Interface and Control

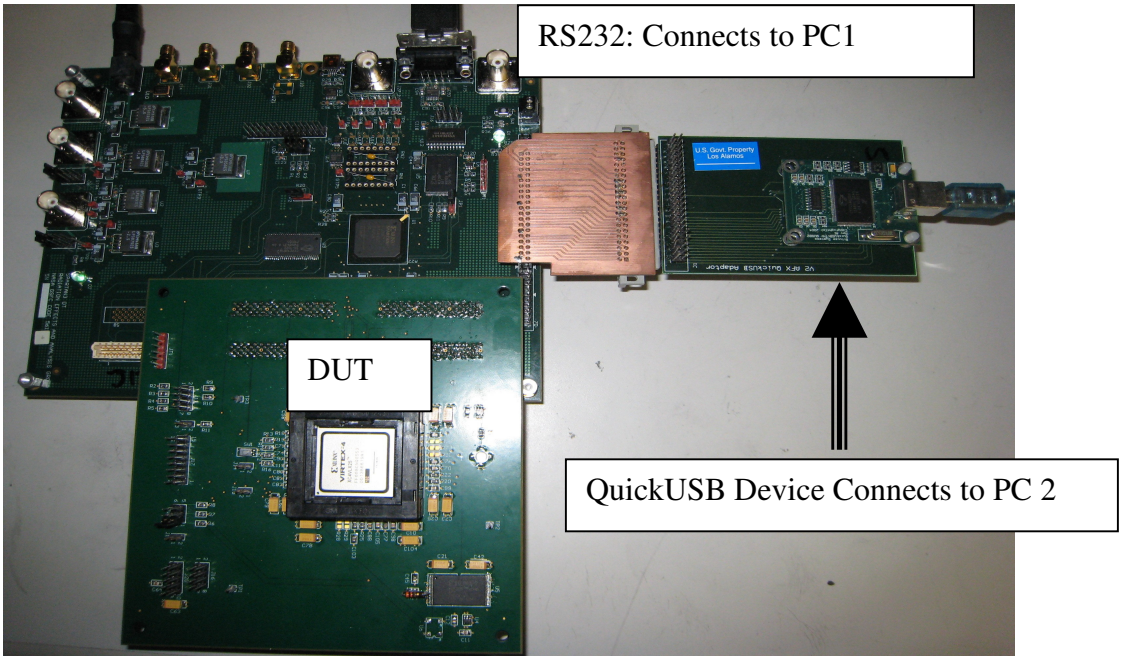

Figure 5: Tester and Xilinx DUT Board

The primary method of which the User controls the tests is via a LABVIEW interface running on a PC (noted as PC1 in Figure 5: Tester and Xilinx DUT Board). PC 1 communicates with the LCDT with a RS232 serial link. The format of communication is a command/Data 4 byte word (see Table 5 : Summary of Commands Used in Virtex-4 LX25 Tester).

Table 5 : Summary of Commands Used in Virtex-4 LX25 Tester

Command #Hex	Command	D0	D1	D2	Description
01	Reset DUT	N	N	N	Resets VIRTEX-4 LX25
02	Start Test	N	N	N	Starts VIRTEX-4 LX25 clock and data generation
90	Pattern Number	Y	N	N	0,1,or checker board
A0	Clock Frequency	Y	N	N	Clock frequency divider of 150mhz
81	Write Configuration Data	N	N	N	PC sends configuration data to Tester via RS232 port. Tester stores data in onboard SRAM

04	Start configuration	N	N	N	Tester configures the LX25 by sending the downloaded configuration data to the LX25 via the SelectMap parallel port.
06	Start Scrub	N	N	N	Scrubbing is turned on
0E	Inject error On	N	N	N	Scrubber will turn on error injection
7A	Scrub Error High	Y	Y	Y	Upper address bound for error inject
79	Scrub Error Low	Y	Y	Y	Lower address bound for error inject
05	Start Readback	N	N	N	Turns readback on
7C	Time Between Readbacks	Y	Y	Y	Time period in ms between each readback. From end of readback to start of next readback
7B	End of Configuration	Y	Y	Y	Memory Location (relative to configuration file) to stop scrubbing – avoids BRAM
89	Set SelectMap Control Register	Y	Y	Y	24 bit value to be placed in control register
8A	Set SelectMap Mask Register	Y	Y	Y	24 bit value to be placed in Mask register
AA	Do Scan	N	N	N	Start the internal scrubber

The following sections are detailed descriptions of commands and their associated functionality.

5.3.1 RESET DUT:

The RESET DUT command is decoded as x01. The following represents the command as noted in Table 5:

x01	xx	xx	xx

Figure 6: Reset Command Format – Command Number, D0, D1, and D2

Once decoded, all DUT inputs will go into reset mode (Reset, CLK_SR and D_SR are low; SelectMap Interface and QuickUSB interface are in reset)

5.3.2 START TEST:

START TEST is decoded as x02. The following represents the command as noted in Table 5:

x02	xx	xx	xx

Figure 7: Start Command Format

All other commands should be supplied before start test. I.e. the user should define the pattern and clock frequency before administering a start. This command activates the CLK_SR and D_SR DUT inputs. DUT must be configured before this command is sent.

5.3.3 PATTERN NUMBER:

There are three data patterns that can be generated by the tester. Data can be a static 0, a static 1, or alternate every VIRTEX-4 LX25 clock cycle (checker board). The command number is x90. The first byte of data (D0) is also decoded (all other bytes are ignored but must be supplied – i.e. all commands must be 4 bytes of data).

x90	x00	xx	xx
x90	x01	xx	xx
x90	x02	xx	xx

Figure 8: Pattern Command Format

D0 decode is as follows:

X00: Static 0
X01: Static 1
X02: Checkerboard Pattern

5.3.4 CLOCK FREQUECY:

The clock frequency command is decoded as xA0. The following represents the command as noted in Figure 9:

xA0	xnn	xx	xx

Figure 9: Clock Frequency Command Format

Upon the receipt of this command, D0 is used as a clock frequency divider. This command must be sent after a RESET DUT and before a START TEST. D0 must be an even number and must

be greater than or equal to 2. The associated output is CLOCK_FREQ. See the LCDT General Tester for more information concerning the processing of CLOCK_FREQ.

5.3.5 Write Configuration Data

5.3.5.1 (old method used in 2006 tests):

The command is decoded as x81. The PC sends the configuration bit file via the RS232 link to the tester. The bit file is generated from Xilinx IMPACT and is actually the ".bin" file. Bin file must be 977488 bytes long.

x81	xx	xx	xx

Figure 10: RS232 Write Configuration Command Format

5.3.5.2 New Method – QuickUSB 2007 Tests

New method of sending data was used in the 2007 test setup. RS232 link takes roughly 85 seconds. We developed a USB controller using the QUICKUSB parallel to serial device. The full data set is now able to be sent under 1 ms.

5.3.6 Start Configuration

The command is decoded as x04. Once the configuration data has been dumped to SRAM (either by RS232 link or QuickUSB link), the tester is able to configure the DUT. Data does not need to be sent to SRAM every time the user wants to configure. Once bin file is stored in SRAM (and SRAM has not been corrupted by a data run or loss of power), then the user can reconfigure repeatedly.

x04	xx	xx	xx

Figure 11: Start Configuration Command Format

5.3.7 Start Scrub

The command is decoded as x06. Starts scrubbing the DUT configuration-memory. DUT must first be configured (along with the corresponding bin file dumped into onboard Tester SRAM).

x06	xx	xx	xx

Figure 12: Scrub Command Format

5.3.8 Inject Error

The command is decoded as x0E. DUT must first be configured (along with the corresponding bin file dumped into onboard Tester SRAM). Start Scrub must be turned on. This command should be used in conjunction with Scrub Error High and Scrub Error low commands. Command will inject error within a range of configuration address spaces. If the Scrub Error High and Scrub Error low commands are not used, Error injection will occur from address x800 to x70000 (relating to actual bin file byte addressing)

.

x0E	xx	xx	xx

Figure 13: Start Injecting Errors Command Format

5.3.9 Scrub Error High

The command is decoded as x7A. Designates the upper bound address of configuration memory error injection. See section 5.3.8.

x7A	MSB	NN	LSB

Figure 14: Error Injection Upper Bound Command Format

Address is 20 bits (19:0). MSB 3:0 is used; MSB 7:4 is unused. NN and LSB 7:0 is used. Address(19:0) = MSB(3:0)NN(7:0)LSB(7:0)

5.3.10 Scrub Error Low

The command is decoded as x79. Designates the lower bound address of configuration memory error injection. See section 5.3.8.

x79	MSB	NN	LSB

Figure 15: Error Injection Lower Bound Command Format

Address is 20 bits (19:0). MSB 3:0 is used; MSB 7:4 is unused. NN and LSB 7:0 is used. Address(19:0) = MSB(3:0)NN(7:0)LSB(7:0)

5.3.11 Start Readback

The command is decoded as x0E. DUT must first be configured (along with the corresponding bin file dumped into onboard Tester SRAM). Start Scrub must be turned on. This command should be used in conjunction with Scrub Error High and Scrub Error low commands. Command will inject error within a range of configuration address spaces. If the Scrub Error High and Scrub Error low commands are not used, Error injection will occur from address x800 to x70000 (relating to actual bin file byte addressing)

.

x05	xx	xx	xx

Figure 16: Start Readback of Configuration Memory Command Format

5.3.12 Time Between Readbacks

The command is decoded as x7C. Designates wait time after a readback has been performed until the next readback will be performed. It is measured in milliseconds and is 24 bits. See section 5.3.11 for start readback command. Time(23:0) = MSB(7:0)NN(7:0)LSB(7:0)

x7A	MSB	NN	LSB

Figure 17: Time between Readbacks Command Format

5.3.13 End of Configuration

The command is decoded as x7B. Designates what byte address (relative to the configuration bin file) to stop scrubbing. Address(19:0) = MSB(3:0)NN(7:0)LSB(7:0)

x7B	MSB	NN	LSB

Figure 18: Last Address Scrub Command Format

5.3.14 Set Control Register and Set Mask Register

The command is decoded as x89 (control register setting) and x8A(Mask Register setting). When scrubbing the Xilinx V4 series, the GLUT MASK bit must be set if SRL or Dynamic RAM is used. Byte 0 can not be changed and is hard-coded in the tester (byte 0 corresponds to the LSByte of the register). Care must be taken because although the bytes are LSByte first, the ordering in the byte is MSB first (7:0).

x89	Byte1	Byte2	Byte3

Figure 19: Control and Mask Register Command Format

5.3.15 Start Scan

The command is decoded as xAA. This command starts the self scrubber. The DUT should be configured via JTAG (no configuration dump via RS232 and QuickUSB) ;do not use the start configuration ; and do not use the start scrub command

.

xAA	xx	xx	xx

Figure 20: Start Readback of Configuration Memory Command Format

5.4 Configuring the DUT via the Tester

Because the Xilinx device has SRAM based configuration, the user must write the configuration memory. We have decided to control the configuration from the tester. See Figure 21: Tester Controlled Configuration Flow Diagram for a flow of configuration:

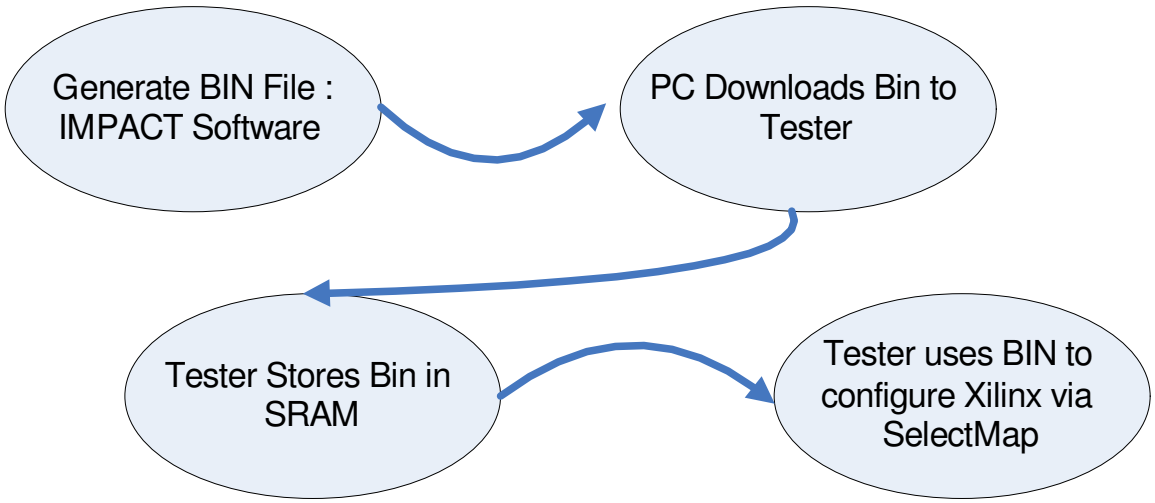

Figure 21: Tester Controlled Configuration Flow Diagram

The tester is connected to SelectMap I/O of the DUT and the mode is set so that the Tester is Master and the DUT is slave. 8 bit SelectMap is used at 30 MHz. Before configuration can be performed, the user must dump the ".bin" file to the tester SRAM. This can be accomplished in 1 of 2 ways:

1. via RS232 cable using the write configuration command: x81 (labview environment). This method uses the computer that is running labview. It is part of the regular command stream.
2. via the QuickUSB set-up including the user interface. This method requires a separate computer that is running the Launch USBmain.exe (quickusb GUI). Write data command

must be set pointing to the bin file. The software will determine the size of the file and send the correct number of words (16 bit transfers @ 50 MHz).

If using the QuickUSB device, the Tester I/O containing quickusb are utilized (connected to the parallel portion of the quickusb device). The serial end of the quickusb device is connected to a USB cable that is plugged into the extra computer. The user must run the Launch USBmain.exe program to invoke the user GUI.

5.5 Processing the DUT Outputs

The outputs of the DUT are fed to the tester for data processing. The objective of the data processing is to synchronously capture data using SHFT_CLK (as a data enable) and SCAN_DATA (as a 4 bit window of DUT Data). SHIFT_CLK has a maximum frequency of 37.5MHZ (150 MHZ divided by 4). It is a control signal indicating new data. It is considered asynchronous to the tester and is sampled using the tester's system clock (max 150 MHZ). Thus, the tester's sampling clock will always be 4 times as fast as SHIFT_CLK. The SHFT_CLK is fed into a metastability filter and an edge detect. This process takes 1 to 2 clock cycles of the sampling clock (detection will be delayed by 1 to 2 sampling clock cycles of the actual edge). Once the edge is detected, data is then sampled and registered. The data is then registered again. The comparison is made against the second registered data and if there is a mismatch, the error is reported.

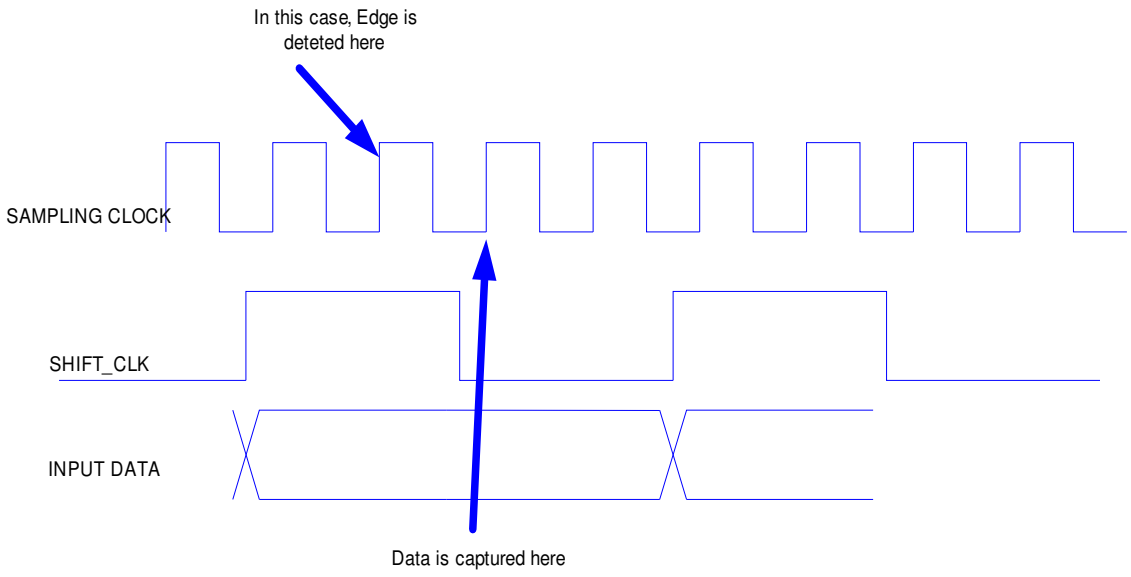

Figure 22: Timing Diagram of Expected DUT Outputs

6. HEAVY ION RESULTS: TEXAS A&M UNIVERSITY 3/2006 TO 7/2006

The VIRTEX-4 LX25 devices were irradiated at 25MeV/u with Argon, and Xenon beams at normal

incidence (0) and 45 degrees (yielding effective LETs of approximately) at the Texas A&M University Cyclotron Single Event Effects Test Facility (please refer to Section **3 Test Facility**). Faults from the VIRTEX-4 LX25 devices were encountered at all LETs at 100 MHZ.

The VIRTEX-4 LX25 devices were tested to measure the Single Event latchup cross section under the above conditions. Each part was placed in the beam until a Single Event latch (SEL) event occurred; 10^7 ions/cm^2 ; or a SEFI occurred – the beam fluence was then recorded. During our experiment, no Single Event latchup events occurred, yielding a threshold SEL LET for latchup of > 55 MeV•cm^2/mg.

The VIRTEX-4 LX25 devices were also tested to measure the error cross section under the above conditions. Each part was placed in the beam until 10^7 ions/cm^2 was reached or a SEFI occurred.

6.1 Cross Section with respect to LET

Data is currently being analyzed. Check back for updated report, or contact Melanie Berg, Melanie.D.Berg@nasa.gov

6.2 Bit Error Rate Calculations

Bit error rate calculations will be performed using the **CREME96** at worst case GEO, the errors-bit/day were:

The flux for ions above Argon was too high resulting in unreliable data. Future tests will sweep the ion cocktail range to Xenon. The Bit error rate calculations will be given at that time.

7. HEAVY ION RESULTS: TEXAS A&M UNIVERSITY 8/2007

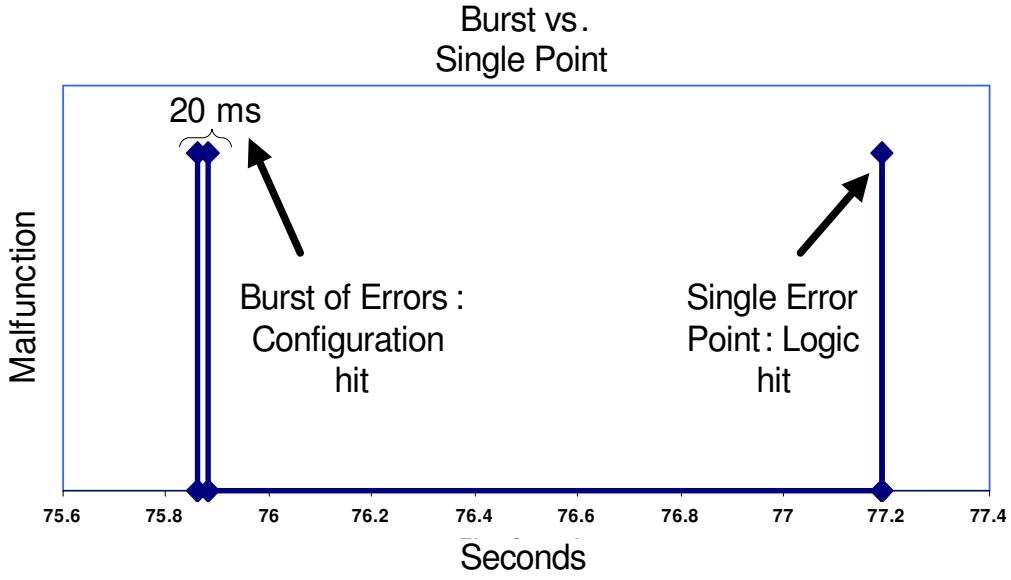

Figure 23: Illustration of Burst vs. Single Point Failures

Figure 23: Illustration of Burst vs. Single Point Failures shows two types of categories of errors:

(1) Burst: Errors occurring for a long period of time
(2) Single Point: error occurring for one clock cycle of the DUT

A category 1 malfunction occurs when a configuration bit gets hit. It can only be corrected upon reconfiguration or scrubbing. In this case, the external scrubber corrected the bit(s) and normal operation resumed after 20ms. A single point failure occurs when the internal logic portion of the FPGA reverses its state due to a radiation strike and the effect is stored within a flip-flop. The implemented function within the DUT allows all single point failures to be overwritten by the next clock cycle (no enables are utilized). This analysis affects design strategy such as mitigation, logic utilization, and time specifications and must be taken into account for flight missions.

When the output of the DUT is stuck in a burst state, other potential errors will be masked. Due to the long duration of bursts, a true cross-section can not be accurately calculated by the traditional method of events divided by fluence. In this case we calculate time in burst per test and subtract an approximate number of particles that would affect the DUT during this period:

$$\sigma = \frac{NE}{TFL - (TB * Flux)}$$

NE: Number of Events

TFL: Total Effective Fluence

TB: Time in Burst

Flux: Approximate reported particle flux (particles/second)

It is important to note, that when we reduce the time in burst (configuration memory errors), the DUT approaches the behavior of an antifuse device (configuration is hardened). However, we do not eliminate the logic errors. They still exist and will be evident as illustrated by the single bit errors in the graph as in Figure 3.

We are performing dynamic testing and are investigating malfunction @ 100MHz with obvservability of every DFF within the device. The probability of incurring a fault is dependent on both the configuration memory and on the device logic. While calculating an error cross section per bit, care must be taken because the probabilities of configuration memory and of DFFs (logic bits) are not the same. In addition, as the technology scales down, multiple bit errors become significant. Simply normalizing the error by total bit count does not take this phenomenon into account. Because of the potential discrepancy, we chose to calculate error cross-section per design malfunction. In this case, errors can only be masked by bursts and are not masked due to complex functionality. The cross section can then be easily adjusted and normalized as demonstrated in section B.

7.1 Cross Section Analysis

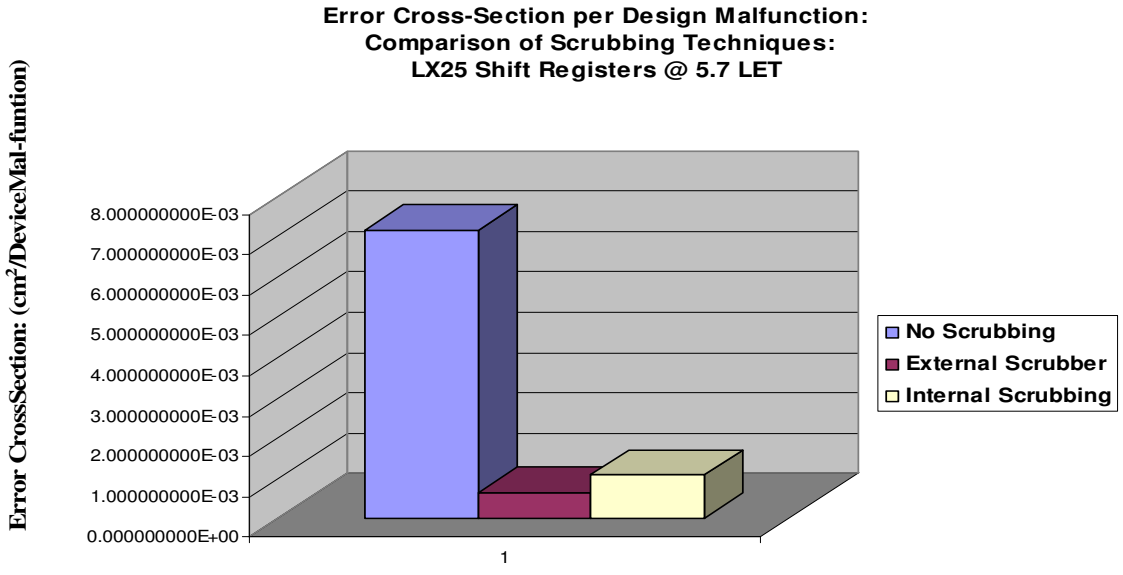

Figure 24: External Scrubbing vs. Internal Scrubbing @ 0 degress Incidence

The difference in performance (error cross-section) between the external vs. internal scrubbers was not as great as expected (see Figure 24: External Scrubbing vs. Internal Scrubbing @ 0 degress Incidence). We assume this is a result of running tests until uncorrectable states occur (SEFI). This cross-section does not reflect time to SEFI, it reflects malfunction during operational time. Accordingly, although the cross-sections did not have a large difference in value, the external scrubbing was always recoverable without the need for a reset or power cycle (for our DUT design), whereas the internal scrubbing was never recoverable – i.e. faults occurred that were uncorrectable. Time to SEFI cross sections will be calculated. We have seen a notable difference in performance between the external scrubber and the internal scrubber within the FX60 Power PC tests performed by our group[8]. More data is currently being analyzed.

7.2 Resource Analysis

The NASA/GSFC Scrubber had the best performance as expected (because it is not dependent on MBU). The external scrubber incurred zero resource errors at the end of each external run as illustrated in Figure 25: Resource Post Irradiation. The external scrubber wrote through BRAM for each test (the design did not use BRAM so this is a valid setting).

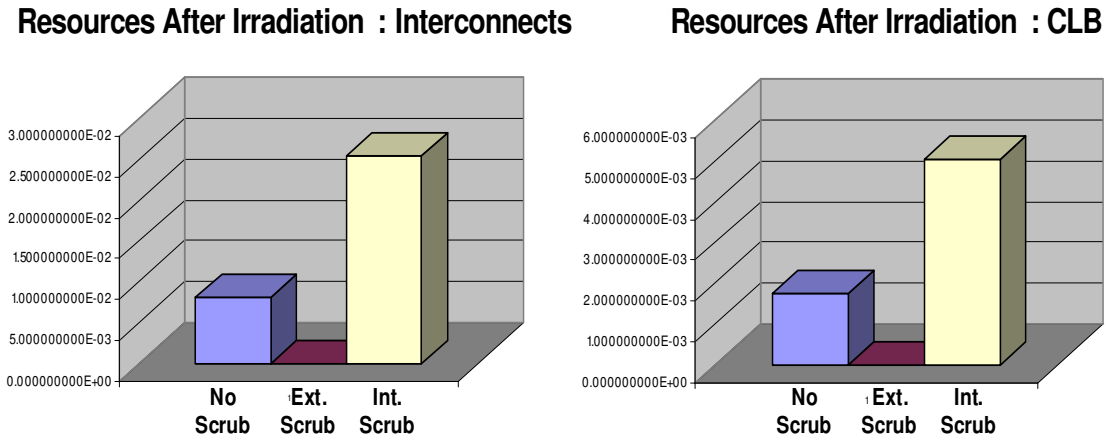

Figure 25: Resource Post Irradiation

It is interesting to note that the readback data from the internal scrubber consistently had a higher count of resource errors. We believe this is due to the fact that we performed readback post test. The tests were terminated if the device entered an uncorrectable state. At this point, the internal scrubber may have written bad data into the frame after miscalculations from the SECDED algorithm.

Data is currently being analyzed from tests that contained intermediate readbacks during irradiation. This will enable the analysis to have a finer granularity of resource observation.

8. PROTON RESULTS 3/2006-7/2006

Limited tests performed due to the lack of samples and time. The following are the results from the separate test proton test trips (please refer to Section 3 Test Facility)

8.1 Proton dose levels (63 MeV protons) of 100 to 200 krads(Si) per device.

No SEUs observed at 15 MHz for any string. Few SEUs observed at worst case 150 MHz. SEU Cross-section of 6.65E-16 cm^2 per device for 4F4L. A SEU Cross-section of 3.5E-15 cm^2 per device for 4F8L has been calculated. There is roughly an order of magnitude confidence level on results (low statistics). There were no SEUs observed on other DUT strings at 150 MHz

8.2 Proton dose levels (195 MeV protons) of 300 krads(Si) per device

There were no SEUs observed at 18.75 MHz for any string. Just a few SEUs observed at worst case 150 MHz. A SEU Cross-section of 8.5E-16 cm^2 was calculated per device for 8F0L and a SEU Cross-section of 2.8E-16 cm^2 was calculated per device for 8F8L

9. PROTON RESULTS: 8/2007

Results are still being analyzed and are dependent on future testing on 10/207

10. FURTHER TEST REQUIREMENTS

Additional Data points (data pattern and frequency, with respect to LET) are needed to fill out the data sets for some of the architectures

10.1 Appendix 1:

See www.xilinx.com and contact Melanie.D.Berg@gsfc.nasa.gov for further details: